

## **PHASE SELECTION MECHANISM FOR OPTIMAL**

### **SAMPLING OF SOURCE SYNCHRONOUS CLOCKING INTERFACE DATA**

#### **Abstract of the Disclosure**

Phase selection mechanisms for the optimal sampling of data at the receiving end  
5 of a SSC interface. The receiver is allowed to choose between several phases of its local  
clock, to best synchronize the transmitter data to the receiver clock domain. It results in a  
minimum depth first in first out (FIFO) register to accomplish the handoff of transmit  
data from the transmit clock to the receive dock. It avoids the requirement of a delay  
locked loop (DLL) to bring the transmitter clock into a desired phase relationship with  
10 respect to the receiver clock. At least one embodiment of the present invention provides  
a solution specific to the DDR or full rate clocking SSC interface.